SUPPORTING CIRCUITRY AND METHOD FOR CONTROLLING PIXELS

CROSS-REFERENCE TO RELATED APPLICATION(S)

[0001] This application is related to U.S. Patent Application No. _____, entitled "METHOD AND SYSTEM FOR SPATIAL-TEMPORAL DITHERING FOR DISPLAYS WITH OVERLAPPING PIXELS" (Attorney Docket No. 371798010US), which is hereby incorporated by reference in its entirety.

FIELD OF THE INVENTION

[0002] This invention relates to visual displays. More particularly, this invention relates to a circuitry for controlling the display of information via a display.

BACKGROUND

[0003] Over the years as computer and related displays have evolved, a need has arisen to convey information on such displays with greater accuracy and clarity, particularly in the field of color displays. Digital information on such display have traditionally been displayed via cathode ray tubes ("CRT") and, as technology progressed, liquid crystal displays ("LCDs") and plasma screen display. Either with a CRT, LCD or plasma screen, digital information is conveyed at a display by way of a pixel. Each pixel has subcomponents (i.e., red, green, and blue) which are also called "subpixels." Various hardware associated with actuating selected desired pixels and subpixels have evolved over the years in an attempt to keep pace with the need and demand for greater clarity and accuracy in conveying displayed information. Liquid crystal display technology in particular has also become more widespread in view of the increased clarity that such displays provide with respect to LCDs, economy of size, as well as other advantages.

[0004] Drawbacks, however, have existed in the prior art. Pixels have typically been divided into vertically disposed red green and blue subpixel lines. This arrangement, however, has had drawbacks in that the human eye does not perceive the color blue with the same clarity as the color red and green, due to a lack of blue receptor sites within the human eye. Various attempts have been made at restructuring the subpixel arrangement of the LCD pixels with the idea in mind of achieving greater clarity and taking into account the human realities of perception. One such arrangement has been proposed by ClairVoyante Labs.

[0005] Even with such structure, however, several drawbacks and problems still exist. Correcting image display problems with attendant supporting circuitry has been attempted, however, such attempts have not produced solutions to many display problems. For example, there remain undesirable image artifacts with such displays, such as losing contrast on every other line, creating undesirable patterns as well a general loss of contrast in the image resulting in non-uniformities of the image depending upon various transient conditions which vary with the imaging process. As such, it would be desirable to provide supporting circuitry which would lend itself to more accurately actuating visual displays, e.g. liquid crystal displays without the undesirable image artifacts and the unintended poorer image quality conditions. The present invention provides a solution to such drawbacks and overcomes many problems associated with poor image display.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] In Figure 1 there is shown a pixel arrangement having five subpixels.

[0007] In Figure 2 there is shown a pixel arrangement having five subpixels.

[0008] In Figure 3 there is shown an integrated circuit layout cross-sectional top plain view of an integrated circuit pixel arrangement.

[0009] In Figure 4 there is shown a circuit diagram of the layout shown in Figure 3.

[0010] In Figure 5 there is shown the timing diagram illustrating various signals occurring in the operation of Figures 4 and 6.

[0011] In Figure 6 there is shown the circuit diagram for the operation of Figures 1, 2 and 3.

[0012] In Figure 7 there is shown a circuit diagram for the operation of Figures 1, 2 and 3.

DETAILED DESCRIPTION

[0013] In Figure 1 there is shown a pixel matrix structure in which a group of subpixels are arranged in a group of five. Such a matrix is proposed by ClairVoyante Labs. It will be appreciated that this pixel structure is organized in rows in a display and is progressively scanned in order to actuate the display. In this structure, the subpixel arrangement includes a generally central 12 generally rectangular subpixel with pentagonal shaped subpixels 14, 16, 18 and 20, disposed about the rectangular subpixel. The subpixel 12 is preferably substantially blue, while subpixels 14 and 20 are generally substantially red in color. Subpixels 18 and 16 are generally substantially green in color. It will be appreciated that different color subpixels are actuated in order to create different selected desired colors. Subpixel 12, being generally blue in color, is bordered by pixels 14, 16, 18 and 20 in order to provide greater perceived visual clarity. Thus, in this arrangement there are five subpixels with a blue generally central subpixel being bordered by juxtaposed generally red and green pixels. As compared to earlier pixel arrangements, this reduces the proportional amount of blue subpixels required, this reducing the number of interconnections without decreasing the perceived sharpness of the images.

[0014] Additional matrixes have been used in which the subpixels have different geometric shapes, such as shown in Figure 2, in which red subpixels 14 and 20 and green subpixels 16 and 18 are disposed adjacent about blue subpixel 12. It will be appreciated that other geometric shapes other than shown in Figures 1 and 2 may also be employed. Such a matrix is also proposed by ClairVoyante Labs.

[0015] Turning now to Figure 3, there is shown a top structural view of a capacitor formed by the pixel electrode forming the dielectric of the capacitor and liquid crystal back plane (BP) the liquid crystal material view of the Figure 1 as an integrated thin film circuit with LCD subcells 34, 43, 51, 56 and 60 integrated with thin film transistors 30, 44, 48, 54, 62 and capacitors 32, 46, 47, 52 and 58.

[0016] Each subpixel has a storage capacitor and thin film transistor associated with it. Thus, subpixel 14 has transistor 30 and storage capacitor 32. Subpixel 16 has transistor 44 and capacitor 47 associated therewith. Subpixel 18 has transistor 48 and a capacitor 46. Subpixel 12 has transistor 62 and storage capacitor 58. Subpixel element 20 has a transistor 54 and a capacitor 52. The storage capacitor and transistor arrangement act as a sample and hold circuit as will be described in more detail with respect to the schematic representation of the integrated circuit. The thin film transistors act as switches conveying a data signal (on or off) by way of data lines (not shown) to the selected desired subpixel element. Gate lines 40 (Gate 1), 42 (Gate 2), 57 (Gate 3), 49 (Gate 4) apply control pulses to the aforereferenced transistors and capacitors.

[0017] The schematic of this structure is represented in Figure 4. The operation thereof is described in conjunction with the timing diagram of Figure 5. With respect to the circuit portion associated with red subpixel element 14, a control pulse is sent via gate line 40 (Gate 1) between t_0 and t_1. That pulse is applied to one terminal of storage capacitor 32. This voltage is dropped across storage capacitor 32 and LCD subcell 34. The pulse in these types of operations is quite high, typically on the order of 25 volts. On the order of five volts is dropped across storage capacitor 32 with the resultant approximately 20 volts still applied at node 31. Other values may be applied and the voltages described herein may be higher or lower. This creates in turn, a voltage across the source and drain of thin film transistor 30 (R1) which in turn, causes a resultant current flow through the transistor. This current flow changes the voltage drop across the liquid crystal cell 34. However, when the next signal is applied by way of line 42 (Gate 2), at the gate of transistor 30, it opens and the data signal applied by line 50 (Data 1)

flows through transistor 30 and nullifies the effect of any leakage current on cell 34.

[0018] Similarly, with respect to the circuitry relevant to green subpixel 18, storage capacitor 46 is coupled to line 40 (Gate 1) which, in turn, delivers a pulse also between t_0 and t_1 which is applied to one electrode of storage capacitor 46 resulting in a voltage change of approximately 20 volts at node 53. This also causes a leakage current and a voltage change at node 53. However, when line 42 (Gate 2) thereafter applies a subsequent pulse between t_1 and t_2 to the gate at transistor 48, this transistor opens and a data signal via data line 55 nullifies the voltage created by the leakage current.

[0019] With respect to the circuit component associated with blue subpixel component 12, storage capacitor 58 receives gate signal 42 (Gate 2) between t_1 and t_2 thereby causing a voltage drop across storage capacitor 58 and LCD cell 60 with a similarly high voltage potential at node 61. A signal from gate line 57 (Gate 3) thereafter opens transistor 62 between t_2 and t_3, which in turn, allows the data signal from data line 49 (Data 2) to flow through transistor 62, to LCD cell 60, thereby also correcting the voltage.

[0020] However, with respect to the circuitry supporting subpixel 16 and 20 (G1 and R2) a different result occurs. The transistor 44 is tied to control line 57 (Gate 3) while the storage capacitor of each subpixel (47 and 52, respectively) is tied to control line 49 (Gate 4) which applies a voltage pulse to the storage capacitor in the time period immediately before the transistor has been opened. As such, the voltage applied by lines 57 and 49 does in fact cause a voltage drop at nodes 45 and 53 due to resultant leakage current. However, because there was a previously applied gate signal, and the data signal from date lines 50 and 55 have already been sent, the leakage current and resultant voltage change, in turn, causes an unintended distorted signal to be applied to LCD subcells 43 and 56 thereby resulting in unintended image artifacts and resultant poorer image quality

[0021] Due to the arrangement of the five subpixel arrangement of Figs. 1 and 2, it will be noted from Figure 3 that the gate lines are arranged in pairs. Gate lines

are paired when they run between two subpixels, (i.e. do not overlap the pixel electrode). As such, the first to be addressed of the gate lines is coupled to the gate of a particular subpixel cells transistor. This leaves a subsequent gate line for connection to the other electrode of the storage capacitor, in other words, the electrode not connected to the LCD cell. Thus, accordingly, as shown in Figure 4, the two lower subpixels circuit portion, namely 16 and 20, have a storage capacitors coupled to the gates of the following pixel gate line. This follows the format of a five pixel arrangement as shown in Figures 1 through 3, but causes the previously described problems and aforereferenced visual artifacts.

[0022] Turning now to the operation of the circuit of Figure 6, there is shown a schematic representation of a supporting circuitry for the liquid crystal display arrangement of Figs. 1 and 2 that avoid the previously described problems. The present invention uses existing gate lines in different order so as to ensure that a switch in the form of a transistor is not opened until after the capacitor associated therewith it is charged so that the data signal then applied corrects any unintended voltage signal applied to the LCD cell thereby minimizing or avoiding altogether unintended image artifacts. The operation is described with respect to the timing diagram of Figure 5. As to the supporting circuitry associated with subpixel 14, transistor 30 of Figure 3 is coupled with data line 50 (Data 1). A storage capacitor 32, in turn, is coupled to gate line 40 (Gate 1) which causes a voltage pulse to the same and LCD cell 34 at pixel node 31. The gate of transistor 30 is coupled to control line 42 (Gate 2). The voltage potential that is applied across the source and drain of transistor 30 in conjunction with voltage on gate line 40 (Gate 1) causes a leakage current and a corresponding voltage change across the liquid crystal cell 34. The control signal sent via control line 42 (Gate 2) that occurs between t_1 and t_2 is coupled to the gate of transistor 30 which, in turn, opens the transistor.

[0023] With respect to the circuit portion relevant to blue subpixel 12, storage capacitor 58 is tied to line 42 (Gate 2) which causes a voltage pulse to the same and LCD cell 60. The pulse applied at line 57 (Gate 3) thereafter opens the gate

of transistor 62. The data signal from data line 49 (Data 2) occurs after the pulse applied by line 42 (Gate 2) and thereby also nullifies any voltage charge against the source and drain of transistor 62 due to leakage current from storage capacitor 58 and LCD cell 60 at node 57.

[0024] Similarly, with respect to the circuit portion pertaining to LCD subpixel 18, storage capacitor 46 is tied to gate line 40 (Gate1) which, in turn, applies a corresponding pulse as shown in Figure 5 between t_0 and t_1. Thereafter, gate line 42 (Gate 2) delivers a pulse to the gate of transistor of 48 between t_1 and t_2, thereby opening same and allowing the data signal from data line 57 (Data 3) through transistor 48 to be applied against LCD subcell 51 but also nullifying the effect of any previous leakage current and the unintended voltage change to the pixel node 53.

[0025] However, as to the circuit portion corresponding to subpixels 16 and 20, a different result occurs and the aforediscribed unintended image artifacts are reduced or avoided. Storage capacitor 47 and LCD cell 43 are coupled to line 42 (Gate 2) which applies the voltage pulse there across between t_1 and t_2 and thereby creating a resultant high voltage at pixel node 45 which, in turn, causes leakage current and a corresponding change in voltage at the pixel node 45. Thereafter, the pulse supplied by way of control line 57 (Gate 3) to the transistor gate of transistor 44 opens the transistor 44 thereby allowing the data signal from data line 50 (Data 1) to flow through transistor 44 thereby nullifying the voltage developed by the previously described leakage current and providing a corrected signal to LCD subcell 43.

[0026] Turning now to the circuitry associated with red subpixel component 20 of Figure 6 while also referring to the timing diagram of Figure 5, it will be seen that storage capacitor 52 is coupled to control line 42 (Gate 2). Thus, capacitor 52 is charged and the voltage is applied against storage capacitor 52 and LCD cell 56 thereby causing leakage current across transistor 54. However, when the signal occurring at line 57 (Gate 3), which occurs after the signal from line 42 (Gate 2), is applied at the gate of transistor 54 thereby opening the transistor, the data

signal from data line 57 (Data 3) flows through transistor 54 and pixel node 71 to LCD cell 56, thereby nullifying the error voltage developed across the source and drain of transistor 54 such that the data signal applied to LCD cell 56 is not disturbed thereby avoiding the unintended image artifacts previously associated with Figure 4.

[0027] The bottom two data signals of Figure 5 illustrate the difference in operation between the circuitry of Figure 4 versus Figure 6 at node 45. The waveforms are not drawn to scale as compared to the signals shown above from lines 40-49 (Gates 1-4). It will thus be appreciated that effect of leakage current and the results and the poorer image quality are reduced thereby.

[0028] In this embodiment, control line 49 (Gate 4), is not used for the first pixel set. An important factor being that an existing pixel structure and the attendant circuitry can be used with different connections thereof such that each capacitor is charged before the attendant transistor is opened to receive the desired data signal. A typical time over which the pattern repeats would be 30 milliseconds.

[0029] In Figure 7 there is shown an alternative embodiment of the present invention by which the unintended image artifacts are obviated or greatly reduced by coupling the storage capacitory to ground as shown herein. Thus, with respect to the circuit component supporting red subpixel element 14 and green subpixel 18, the performance of this circuit is similar to that described before, with no artifacts. However, with respect to the other two circuit components 16 and 20, the performance is different in that no pulse is seen across the storage capacitor, so no leakage current can occur. More specifically, storage capacitors 47 and 52 are tied to ground, such that they never couple a voltage pulse to the tranistors 44 and 54 and thus no leakage current occurs. As such, when the data signals from data lines 50 (Data 1) and 57 (Data 3) are sent, there is no preexisting leakage current whose effects must be nullified and the unintended aforedescribed image distortions are thus avoided or greatly reduced.

[0030] It will be appreciated that the above described circuitry is only one way of achieving the aspects of the present invention, and that many alternative circuits

may be designed by those skilled in the art, an important factor being an awareness of the timing and the elimination of undesirable leakage voltage through the corresponding transistor and the attendant undesirable image artifacts.

[0031] It will be further appreciated in view of the aforereferenced description, that devices such as televisions, computers, electronic notebooks and other devices that utilize visual displays can benefitted through use of the present invention. It will be further appreciated that the problems associated with the prior art can be avoided while still using the aforedescribed pixel structure of Figures 1, 2 and 3 yet with modifications that, in turn, can be manufactured by utilizing existing gate lines of such pixel structure in different orders.

[0032] The above detailed descriptions of embodiments of the invention are not intended to be exhaustive or to limit the invention to the precise form disclosed above. While specific embodiments of, and examples for, the invention are described above for illustrative purposes, various equivalent modifications are possible within the scope of the invention, as those skilled in the relevant art will recognize. For example, while steps are presented in a given order, alternative embodiments may perform routines having steps in a different order. The teachings of the invention provided herein can be applied to other systems, not necessarily the system described herein. These and other changes can be made to the invention in light of the detailed description. The elements and acts of the various embodiments described above can be combined to provide further embodiments.

[0033] These and other changes can be made to the invention in light of the above detailed description. In general, the terms used in the following claims, should not be construed to limit the invention to the specific embodiments disclosed in the specification, unless the above detailed description explicitly defines such terms. Accordingly, the actual scope of the invention encompasses the disclosed embodiments and all equivalent ways of practicing or implementing the invention under the claims.

[0034] Unless the context clearly requires otherwise, throughout the description and the claims, the words "comprise," "comprising," and the like are to be construed in an inclusive sense as opposed to an exclusive or exhaustive sense; that is to say, in a sense of "including, but not limited to." Words using the singular or plural number also include the plural or singular number respectively. Additionally, the words "herein," "above," "below," and words of similar import, when used in this application, shall refer to this application as a whole and not to any particular portions of this application. When the claims use the word "or" in reference to a list of two or more items, that word covers all of the following interpretations of the word: any of the items in the list, all of the items in the list and any combination of the items in the list.

[0035] While certain aspects of the invention are presented below in certain claim forms, the inventors contemplate the various aspects of the invention in any number of claim forms. For example, while only one aspect of the invention is recited as embodied in a semiconductor chip, other aspects may likewise be embodied in a chip. Accordingly, the inventors reserve the right to add additional claims after filing the application to pursue such additional claim forms for other aspects of the invention.

[0036] From the foregoing, it will be appreciated that specific embodiments of the invention have been described herein for purposes of illustration, but that various modifications may be made without deviating from the spirit and scope of the invention. Accordingly, the invention is not limited except as by the appended claims.